

FIG. 3 is a block diagram of a system 10' according to one embodiment of the present invention. The system 10' includes a first input 14, a first output 12, a second input 18a, a second output 18b, a first processing unit 60, a second processing unit 62, a third processing unit 64, a fourth processing unit 66, a fifth processing unit 68, a sixth processing unit 70, a seventh processing unit 72, and an eighth processing unit 74. The first input 14 is connected to the first processing unit 60. The first output 12 is connected to the first processing unit 60. The second input 18a is connected to the second processing unit 62. The second output 18b is connected to the second processing unit 62. The third processing unit 64 is connected to the fourth processing unit 66. The fifth processing unit 68 is connected to the sixth processing unit 70. The seventh processing unit 72 is connected to the eighth processing unit 74.

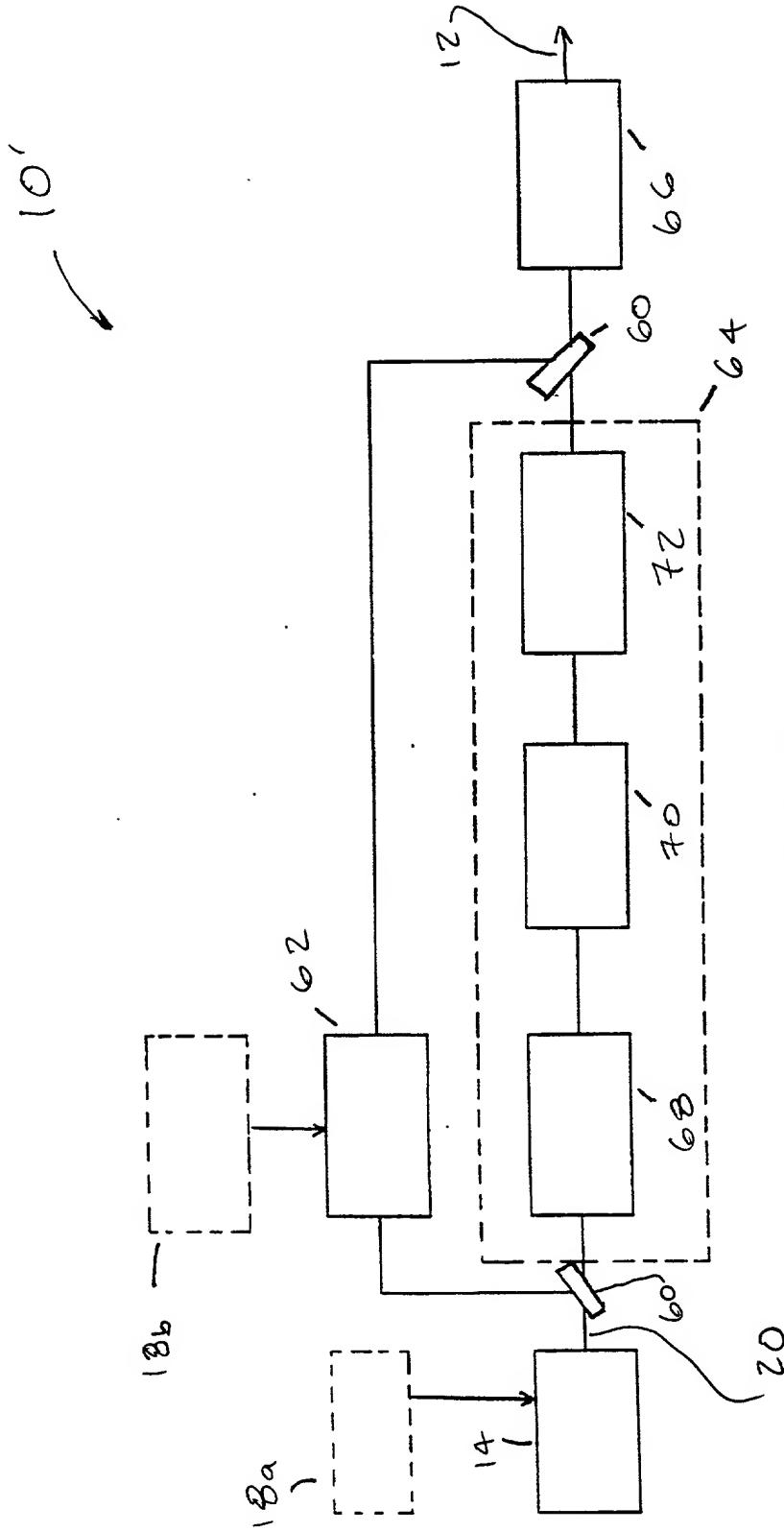


FIG. 3